**EE 310 – Lab 3 Report**

**NAU, 21 February 2020**

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**Problem Description**

In this lab, we are going to design a 4-bit multi-function register circuit. It will be capable of clearing, incrementing, decrementing and adding a value onto the current value of the register.

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Figure 1. Expected behavior of the circuit

**Solution Plan**

In order to solve the problem explained above, I have *broken down the problem into a switch case so on the codintion of X and S the math for the certain case is calculated but not actually saved until the clock hits a positive edge. Then it is output on the 7 segment display.*

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Figure 2. State diagram for the proposed solution

**Implementation and Test Plan**

I have implemented the solution plan explained above, by *the code is exactly what I set out to do and worked first try.*

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| // Lab3 module  module lab3 (clk, S, X, Q, SS);  input clk;  input [3:0] X;  input [1:0] S;  output reg [6:0] SS;  output reg [3:0] Q = 0;  reg [3:0] D = 4'b0000;  always @ ( X , S ) begin // new input  case(S)  2'b00 : D = Q + 1;  2'b01 : D = 4'b0000;  2'b10 : D = Q - 1;  2'b11 : D = Q + X;  endcase  end  always @( posedge clk ) begin //at posedge  Q = D;//at clock set new Q  case ( Q )  4'b0000 : SS = 7'b1000000 ;  4'b0001 : SS = 7'b1111001 ;  4'b0010 : SS = 7'b0100100 ;  4'b0011 : SS = 7'b0110000 ;  4'b0100 : SS = 7'b0011001 ;  4'b0101 : SS = 7'b0010010 ;  4'b0110 : SS = 7'b0000010 ;  4'b0111 : SS = 7'b1111000 ;  4'b1000 : SS = 7'b0000000 ;  4'b1001 : SS = 7'b0010000 ;  4'b1010 : SS = 7'b0001000 ;  4'b1011 : SS = 7'b0000011 ;  4'b1100 : SS = 7'b1000110 ;  4'b1101 : SS = 7'b0100001 ;  4'b1110 : SS = 7'b0000110 ;  4'b1111 : SS = 7'b0001110 ;  endcase  end  endmodule  //--------------------------------------------------------------------------//  // Title: baseline\_pinout.v //  // Rev: Rev 1.0 //  // Last Revised: 10/13/2015 by Geraldine Baniqued //  //--------------------------------------------------------------------------//  // Description: Baseline design file contains Cyclone V GX Starter Kit //  // Board pins and I/O Standards. //  //--------------------------------------------------------------------------//  //Copyright 2012 Altera Corporation. All rights reserved. Altera products  //are protected under numerous U.S. and foreign patents, maskwork rights,  //copyrights and other intellectual property laws.  //  //This reference design file, and your use thereof, is subject to and  //governed by the terms and conditions of the applicable Altera Reference  //Design License Agreement. By using this reference design file, you  //indicate your acceptance of such terms and conditions between you and  //Altera Corporation. In the event that you do not agree with such terms and  //conditions, you may not use the reference design file. Please promptly  //destroy any copies you have made.  //  //This reference design file being provided on an "as-is" basis and as an  //accommodation and therefore all warranties, representations or guarantees  //of any kind (whether express, implied or statutory) including, without  //limitation, warranties of merchantability, non-infringement, or fitness for  //a particular purpose, are specifically disclaimed. By making this  //reference design file available, Altera expressly does not recommend,  //suggest or require that this reference design file be used in combination  //with any other product not provided by Altera  //----------------------------------------------------------------------------  //`define ENABLE\_DDR2LP  //`define ENABLE\_HSMC\_XCVR  //`define ENABLE\_SMA  //`define ENABLE\_REFCLK  //`define ENABLE\_GPIO  module baseline\_c5gx(  ///////// ADC ///////// 1.2 V ///////  output ADC\_CONVST,  output ADC\_SCK,  output ADC\_SDI,  input ADC\_SDO,  ///////// AUD ///////// 2.5 V ///////  input AUD\_ADCDAT,  inout AUD\_ADCLRCK,  inout AUD\_BCLK,  output AUD\_DACDAT,  inout AUD\_DACLRCK,  output AUD\_XCK,  ///////// CLOCK /////////  input CLOCK\_125\_p, ///LVDS  input CLOCK\_50\_B5B, ///3.3-V LVTTL  input CLOCK\_50\_B6A,  input CLOCK\_50\_B7A, ///2.5 V  input CLOCK\_50\_B8A,  ///////// CPU /////////  input CPU\_RESET\_n, ///3.3V LVTTL  `ifdef ENABLE\_DDR2LP  ///////// DDR2LP ///////// 1.2-V HSUL ///////  output [9:0] DDR2LP\_CA,  output [1:0] DDR2LP\_CKE,  output DDR2LP\_CK\_n, ///DIFFERENTIAL 1.2-V HSUL  output DDR2LP\_CK\_p, ///DIFFERENTIAL 1.2-V HSUL  output [1:0] DDR2LP\_CS\_n,  output [3:0] DDR2LP\_DM,  inout [31:0] DDR2LP\_DQ,  inout [3:0] DDR2LP\_DQS\_n, ///DIFFERENTIAL 1.2-V HSUL  inout [3:0] DDR2LP\_DQS\_p, ///DIFFERENTIAL 1.2-V HSUL  input DDR2LP\_OCT\_RZQ, ///1.2 V  `endif /\*ENABLE\_DDR2LP\*/  `ifdef ENABLE\_GPIO  ///////// GPIO ///////// 3.3-V LVTTL ///////  inout [35:0] GPIO,  `else  ///////// HEX2 ///////// 1.2 V ///////  output [6:0] HEX2,  ///////// HEX3 ///////// 1.2 V ///////  output [6:0] HEX3,  `endif /\*ENABLE\_GPIO\*/  ///////// HDMI /////////  output HDMI\_TX\_CLK,  output [23:0] HDMI\_TX\_D,  output HDMI\_TX\_DE,  output HDMI\_TX\_HS,  input HDMI\_TX\_INT,  output HDMI\_TX\_VS,  ///////// HEX0 /////////  output [6:0] HEX0,  ///////// HEX1 /////////  output [6:0] HEX1,  ///////// HSMC ///////// 2.5 V ///////  input HSMC\_CLKIN0,  input [2:1] HSMC\_CLKIN\_n,  input [2:1] HSMC\_CLKIN\_p,  output HSMC\_CLKOUT0,  output [2:1] HSMC\_CLKOUT\_n,  output [2:1] HSMC\_CLKOUT\_p,  inout [3:0] HSMC\_D,  `ifdef ENABLE\_HSMC\_XCVR  input [3:0] HSMC\_GXB\_RX\_p, /// 1.5-V PCML  output [3:0] HSMC\_GXB\_TX\_p, /// 1.5-V PCML  `endif /\*ENABLE\_HSMC\_XCVR\*/  inout [16:0] HSMC\_RX\_n,  inout [16:0] HSMC\_RX\_p,  inout [16:0] HSMC\_TX\_n,  inout [16:0] HSMC\_TX\_p,  ///////// I2C ///////// 2.5 V ///////  output I2C\_SCL,  inout I2C\_SDA,  ///////// KEY ///////// 1.2 V ///////  input [3:0] KEY,  ///////// LEDG ///////// 2.5 V ///////  output [7:0] LEDG,  ///////// LEDR ///////// 2.5 V ///////  output [9:0] LEDR,  `ifdef ENABLE\_REFCLK  ///////// REFCLK ///////// 1.5-V PCML ///////  input REFCLK\_p0,  input REFCLK\_p1,  `endif /\*ENABLE\_REFCLK\*/  ///////// SD ///////// 3.3-V LVTTL ///////  output SD\_CLK,  inout SD\_CMD,  inout [3:0] SD\_DAT,  `ifdef ENABLE\_SMA  ///////// SMA ///////// 1.5-V PCML ///////  input SMA\_GXB\_RX\_p,  output SMA\_GXB\_TX\_p,  `endif /\*ENABLE\_SMA\*/  ///////// SRAM ///////// 3.3-V LVTTL ///////  output [17:0] SRAM\_A,  output SRAM\_CE\_n,  inout [15:0] SRAM\_D,  output SRAM\_LB\_n,  output SRAM\_OE\_n,  output SRAM\_UB\_n,  output SRAM\_WE\_n,  ///////// SW ///////// 1.2 V ///////  input [9:0] SW,  ///////// UART ///////// 2.5 V ///////  input UART\_RX,  output UART\_TX  );  lab1 dut( KEY[0] , SW[0] , HEX3 , HEX2 , HEX1 , HEX0 ) ;  endmodule |

Figure 3. Verilog code for the proposed solution

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Figure 5. Lab pictures of the running solution